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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/429,446	10/28/1999	LYNDON W. GRAHAM	SEM4492P0771	5945

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EXAMINER
LEADER, WILLIAM T

ART UNIT	PAPER NUMBER
1741	2

DATE MAILED: 02/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

MF-21

Office Action Summary	Application No.	Applicant(s)
	09/429,446	Graham et al
	Examiner	Group Art Unit
	William Leader	1741

—The MAILING DATE of this communication appears on the cover sheet beneath the correspondence address—

Peri d for Response

A SHORTENED STATUTORY PERIOD FOR RESPONSE IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a response be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for response is specified above, such period shall, by default, expire SIX (6) MONTHS from the mailing date of this communication .
- Failure to respond within the set or extended period for response will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).

Status

☒ Responsive to communication(s) filed on 1/22/2002 with a COM dated 12/13/2001.

☐ This action is **FINAL.**

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle,* 1935 C.D. 1 1; 453 O.G. 213.

Disp sition of Claims

☒ Claim(s) 15-34 is/are pending in the application.

Of the above claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) 15-34 is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claim(s) _____ are subject to restriction or election requirement.

Application Papers

☐ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The proposed drawing correction, filed on _____ is ☐ approved ☐ disapproved.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119 (a)-(d)

☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 11 9(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____.

☐ received in this national stage application from the International Bureau (PCT Rule 1 7.2(a)).

*Certified copies not received: _____.

Attachment(s)

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 20

☐ Interview Summary, PTO-413

☒ Notice of References Cited, PTO-892

☐ Notice of Informal Patent Application, PTO-152

☐ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Other _____

Office Action Summary

The request for continued examination (RCE) filed on January 22, 2002, with a certificate of mailing dated December 13, 2001, is acknowledged.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103© and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jorne et al (6,132,587) in view of Inoue et al (5,556,814), Erb (6,107,186) or Taylor et al (6,203,684), and further in view of Reid et al (6,074,544), Shue et al

(6,140,241) or the Lowenheim text, *Electroplating*.

The Jorne et al patent discloses a process for uniformly electroplating a metal onto a semiconductor wafer. As shown in figure 1, the wafer 1 is held face down opposite anode 2 and brought into contact with electroplating solution which is circulated to the electroplating chamber by pump 26. Power is applied to the wafer by contacts 9. Jorne et al disclose that copper may be electroplated (column 2, lines 63-65).

Applicant has amended claim 15 to recite that the metal is deposited into submicron features and that the surface is prepared with a metal seed layer no more than 1000 Angstroms thick. Both of these limitations are taught by Jorne. At column 2, lines 23-24, Jorne refers to the sub-0.25μm technology. This clearly suggests submicron features as now recited by applicant. At column 2, line 60, Jorne discloses the use of a copper seed layer with a thickness in the range of 500-1000 Angstroms. This range overlaps that now recited by applicant.

The process of claim 15 differs from that of Jorne et al by reciting that the electroplating solution includes ions and/or complexes of a noble metal that is to be plated, and by reciting use of a low current density for a first time period and a higher current density for a second time period.

The Inoue et al patent is directed to forming wiring for integrated circuits on a semiconductor wafer by electroplating. The electroplated metal may be copper,

gold, platinum or palladium (column 6, lines 34-38).

The Erb patent is directed to the formation of a high-density metallization pattern in a semiconductor substrate. Erb discloses that metals employed include copper, gold and silver (column 1, lines 31-34). Erb further discloses that the openings into which the metal is deposited have widths of about 0.8-2.0μm an depths of about 0.3-2.5μm (column 3, lines 30-35). These disclosed ranges suggest the sub-micron range now recited by applicant.

The Taylor et al patent is directed to the metallization of a semiconductor. At column 10, lines 48-52, Taylor et al teach that suitable metals include copper, silver and gold. At column 4, lines 53-55, Taylor et al teach that the small trenches prepared in the damascene metallization process are typically less than 1-2 micrometers in breadth and depth.

Reid et al is directed to a process for electroplating a metal layer onto a semiconductor wafer. Reid teaches that nonuniform deposition resulting from the "terminal effect" may be overcome by first plating with a relatively low current until the resistive drop is negligible, and then increasing the current to improve the plating rate. See the abstract.

The Shue et al patent is directed to the electrochemical deposition of copper metallurgy on an integrated circuit. The deposition is performed in two stages. In the first stage a low current density which provides good coverage is used. After a

brief dwell period wherein the plating current is stopped, a high current density is applied to fill the contacts/vias at a high deposition rate. See the abstract.

The Lowenheim text discloses a process for plating on nonconductors. A thin conductive layer is initially formed on the substrate. Since the conductivity of this layer is low, electroplating is started at a low current density until a fair thickness of electrodeposit is built up, and then a higher current density is used. See page 418.

The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have deposited a noble metal such as platinum using an electroplating apparatus and method such as that disclosed by Jorne et al because noble metals such as platinum, palladium, gold and silver are recognized as an equivalent to copper for the metallization of a semiconductor as shown by Inoue et al, Erb and Taylor et al, and to have used a low current density for a first period of time followed by a higher current density for a second period of time as taught by Reid et al, Shue et al, and Lowenheim because a better filling of surface features and more uniform deposition without burning the initial conductive seed layer would have been obtained.

Claims 16-19 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jorne et al (6,132,587) in view of Inoue et al (5,556,814), Erb

(6,107,186) or Taylor et al (6,203,684), and further in view of Reid et al (6,074,544), Shue et al (6,140,241) or the Lowenheim text, *Electroplating* as applied to claims 15 and 20 above, and additionally in view of Ting et al (6,077,412) and Young et al (4,705,606).

Claims 16, 17 and 19 relate to a step of prerinsing while claims 32-34 relate to a step of precleaning. The Ting et al patent is directed to apparatus and method for electrolytically processing a wafer. Ting et al disclose that the wafer can be washed and dried within processing chamber 10 prior to introduction of the electrolyte (column 13, lines 46-48). During rinsing and drying cycles, the wafer is spun at a relatively high rpm (column 14, lines 13-17). Deionized water may be used (column 14, lines 17-19). Ting et al does not specify that in the cleaning step, an acidic solution should be used as recited in claims 17 and 34. The Young et al patent is directed to a process for depositing metallic interconnections for integrated circuits on a semiconductor wafer and discloses the use of acid in preliminary cleaning. See the surface preparation section of column 3. It would have been obvious at the time the invention was made to have precleaned a semiconductor substrate prior to plating by contacting with water or an acidic solution to have removed contaminants as taught by Ting et al and Young et al. Instant claim 18 recites removing excess plating solution by spinning. While Ting et al disclose the use of spinning to remove liquid from the wafer being treated, plating solution is

not specifically mentioned. However, since Ting et al shows that spinning is effective to remove liquid, one of ordinary skill in the art would have recognized that spinning would have been effective in removing excess plating solution.

Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jorne et al (6,132,587) in view of Inoue et al (5,556,814), Erb (6,107,186) or Taylor et al (6,203,684), and further in view of Reid et al (6,074,544), Shue et al (6,140,241) or the Lowenheim text, *Electroplating* as applied to claims 15 and 20 above, and additionally in view of Abys (4,427,502) and Dubin et al (5,972,192).

Claims 21-26 relate to process parameters used in the electrodeposition of platinum. The Abys patent is directed to a process for electroplating platinum and platinum alloys. The platinum concentration ranges from 0.005 molar to saturation (column 4, lines 40-41). This range includes the range recited in instant claim 21. The pH is preferably within the range of 10 to 12.5 (column 3, lines 53-57). This range includes the range of 11-12 recited in claim 24. Abys discloses that a preferred temperature range is 50 to 70°C. This range falls within the range of 40-80°C recited in claim 22. Abys discloses the use of a broad current range (column 4, lines 43-45) but does not specify that pulsed current should be used. Dubin et al disclose that pulse current as recited in instant claim 25 may advantageously be used in electroplating into the surface features of a semiconductor wafer. See the

abstract. It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Abys to metallize a semiconductor wafer because these parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Dubin et al because it is effective in filling surface features of a semiconductor wafer. Choice of current density would have been a matter of routine optimization within the skill of the ordinary worker in the art.

Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jorne et al (6,132,587) in view of Inoue et al (5,556,814), Erb (6,107,186) or Taylor et al (6,203,684), and further in view of Reid et al (6,074,544), Shue et al (6,140,241) or the Lowenheim text, *Electroplating* as applied to claims 15 and 20 above, and additionally in view of Lowenheim and Dubin.

Claims 27-31 relate to process parameters used in the deposition of platinum. Lowenheim discloses a number of different electroplating baths for the deposition of platinum (page 300). Bath "S" has a pH of 2 which falls within the range recited in instant claim 27. The platinum concentration of this bath is 5 g/l which falls within the range recited in instant claim 28. Lowenheim does not specify the use of pulsed current. Dubin et al disclose that pulse current as recited in instant claim 29 may advantageously be used in electroplating into the surface features of a

semiconductor wafer. See the abstract. It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Lowenheim to metallize a semiconductor wafer because these parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Dubin et al because it is effective in filling surface features of a semiconductor wafer. Choice of current density would have been a matter of routine optimization within the skill of the ordinary worker in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William Leader, whose telephone number is (703) 308-2530. The examiner can normally be reached Mondays-Fridays from 7:30 AM to 3:30 PM eastern time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King can be reached at (703) 308-1146. The fax phone number for *official* after final faxes is (703) 872-9311. The fax phone number for all other *official* faxes is (703) 872-9310. Unofficial communications to the Examiner should be faxed to (703) 305-7719.

Any inquiry of a general nature or relating to the status of this application should be directed to the receptionist whose telephone number is (703) 308-0661.

William Leader:wtl
February 20, 2002

Donald R Valentine

DONALD R. VALENTINE
PRIMARY EXAMINER
GROUP 1700
1741